I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date shown below.

Dated: March 22, 2004 Signature: _____
Paul B. Stephens

Docket No.: 30320/17593
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Murthi Nanja

Application No.: 10/736,728

Filed: December 16, 2003

Art Unit: To be assigned

For: PERFORMANCE MONITORING BASED DYNAMIC VOLTAGE AND FREQUENCY SCALING

Examiner: To be assigned

INFORMATION DISCLOSURE STATEMENT (IDS)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to 37 CFR 1.56, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached Form PTO-1449. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

A copy of each reference on Form PTO-1449 is attached.

This Information Disclosure Statement is filed before the mailing date of a first Office Action on the merits as far as is known to the undersigned. Accordingly, no fee is due. The Commissioner is hereby authorized to charge any fees which may be required to Deposit Account No. 13-2855. A duplicate of this paper is enclosed.

Dated: March 22, 2004

Respectfully submitted,

By _____
Paul B. Stephens
Registration No.: 47,970
MARSHALL, GERSTEIN & BORUN LLP
233 S. Wacker Drive, Suite 6300
Sears Tower
Chicago, Illinois 60606-6357
(312) 474-6300
Attorney for Applicant

Form PTO-1449 (Modified)	Atty. Docket No. 30320/17593	Serial No. 10/736,728
INFORMATION DISCLOSURE STATEMENT	Applicant(s) Murthi Nanja	
	Filing Date December 16, 2003	Art Unit To be assigned

U.S. PATENT DOCUMENTS

Examiner Initials	Document Number	Issue or Publication Date	Name	Class	Subclass	Filing Date (If Appropriate)

FOREIGN PATENT DOCUMENTS

Examiner Initials	Document Number	Publication Date	Country	Translation Yes	Translation No

OTHER DOCUMENTS

	Pering et al., "Dynamic Voltage Scaling and the Design of a Low-Power Microprocessor System", University of California Berkeley, Electronics Research Laboratory, 6 pages (1998)
	Govil et al., "Comparing Algorithms for Dynamic Speed-Setting of a Low-Power CPU", Computer Science Division University of California, pp 13-26 (1995)
	Grunwald et al., "Policies for Dynamic Clock Scheduling", Department of Computer Science University of Colorado, 14 pages (2000)

EXAMINER:	DATE CONSIDERED: